

[illegible]

CLK-GEN
ICS 952801

Page 2

HOST 200MHz
ZCLK 133MHz
AGP 66MHz
PCI 33MHz
USB 48MHz
REF 14.318MHz

3V/5V

Page 22

3V_ALWAYS
5VPCU
3V_S5
1.8V_S5
3VSUS
5VSUS
+3V
+5V
15V

2.5V/1.25V

Page 23

2.5VSUS
1.25VREF
+2.5V
DDR_VTT

**1.2V/1.5V
1.8V**

Page 24

+1.2V_HT
+1.5V
+1.8V

CPU CORE

Page 25

VCC_CORE

**BATTERY
CHARGER**

Page 26

DDR SO-DIMM

Page 5

DDR 333

CPU
AMD Athlon64
SMT uPGA754

Page 3,4

HyperTransport
16x16
1600MT/s

NB
SIS M760GX
(698 PIN BGA)

Page 6,7,8

MuTIOL(1GB/s)

HDD
Primary Master

Page 19

ATA 66/100

ODD
Secondary Master

Page 19

ATA 66/100

USB
3x connector

Page 15

USB 2.0

MINI USB
(BLUETOOTH)

Page 15

SB
SIS 963L
(371 PIN BGA)

Page 11,12,13

Int. Keyboard
87-Key

Page 21

Touch Pad
6-Button

Page 21

EC
NS PC97551

Page 20

LPC

Thermal
Thermal sensor & Fan

ZL5
Block Diagram

RGB

INTA#

DVO

LVDS Transmitter
SIS302ELV

Page 9

LVDS

CRT
1x D-SUB 15-Pin

Page 10

LCD
15" XGA/WXGA

Page 10

REQ0#, GNT0#
INTB#, INTC# IDSEL : AD22

Mini PCI
WLAN 802.11A/G

Page 15

Antenna

REQ1#, GNT1#
INTD# IDSEL : AD17

CardBus
TI PCI1410

Page 14

PC Card
1x type-I/II

MII

LAN PHY
RTL8201CP

Page 16

Transformer

Page 16

RJ-45

Page 16

AC'97 2.1

MDC1.5
56K MODEM

Page 17

RJ-11

Page 16

AC97 Codec
ALC203

Page 17

MIC-In Jack

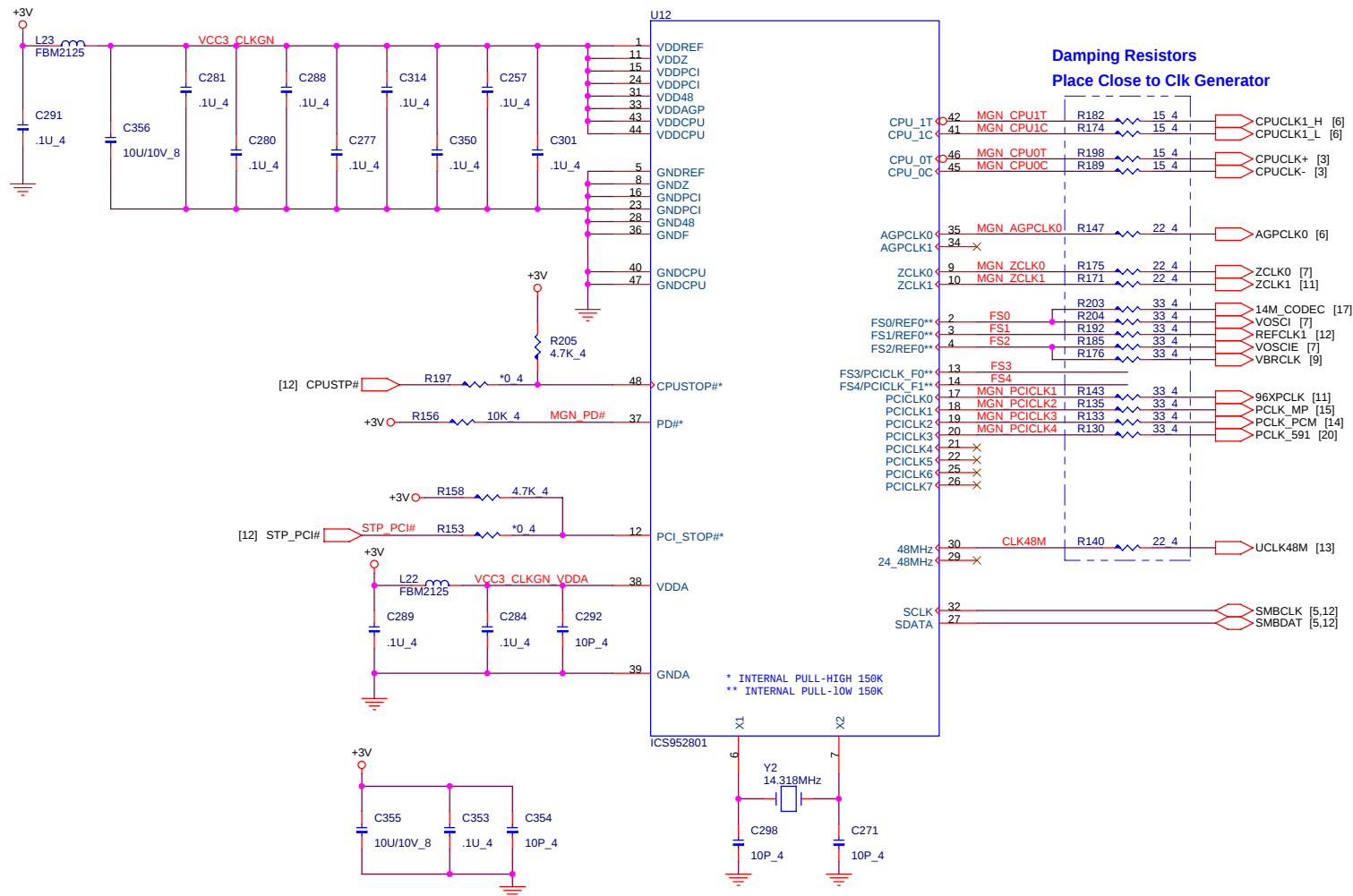
Line-In Jack

AMP
MAX9755

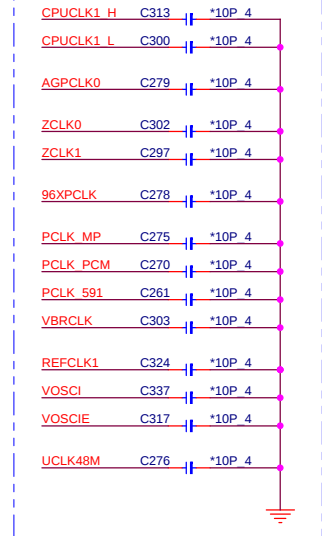
Page 18

HP-Out Jack

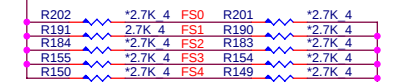
Int. Speaker



By-Pass Capacitors Place Close to Clock Generator



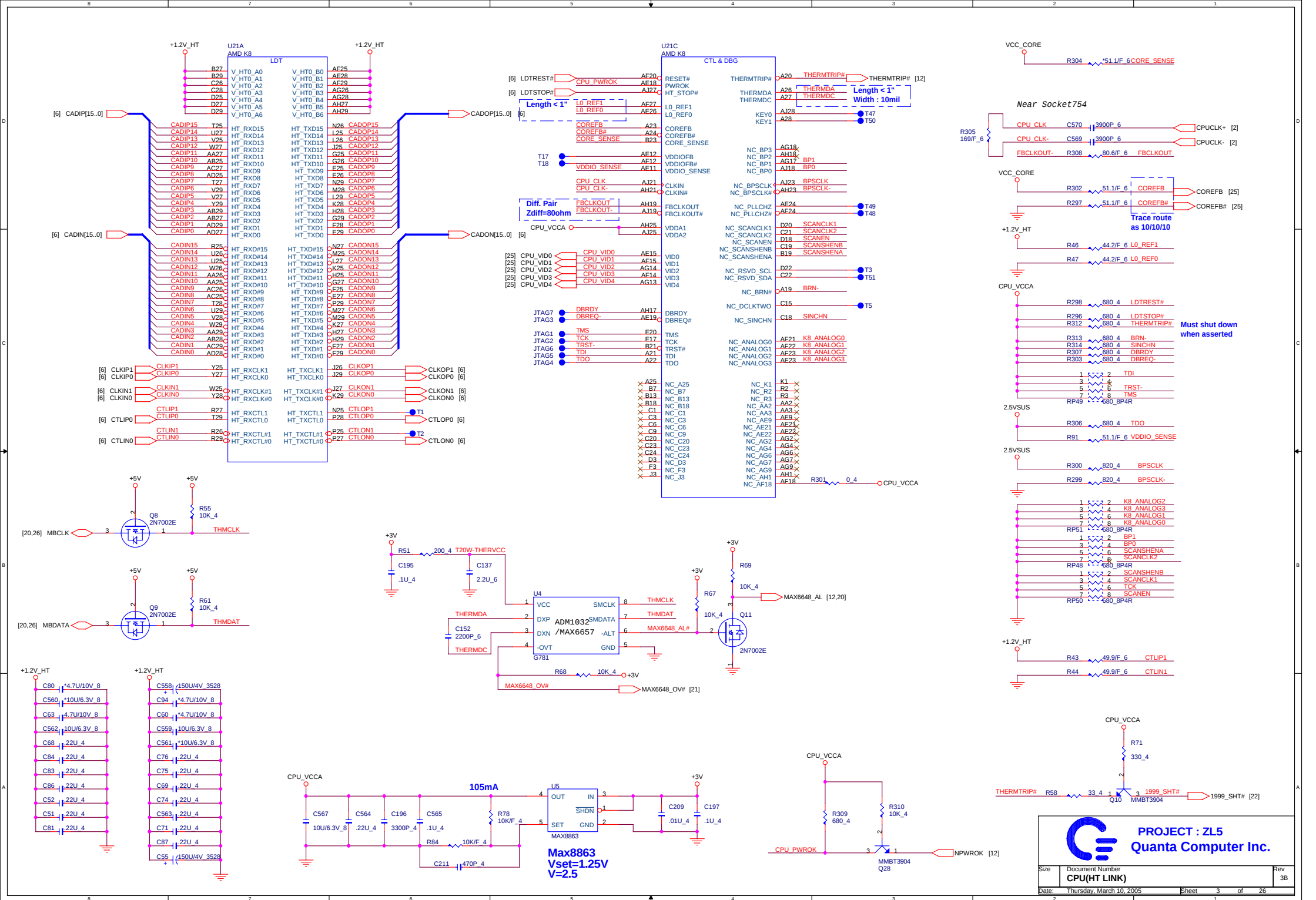
Frequency Selection



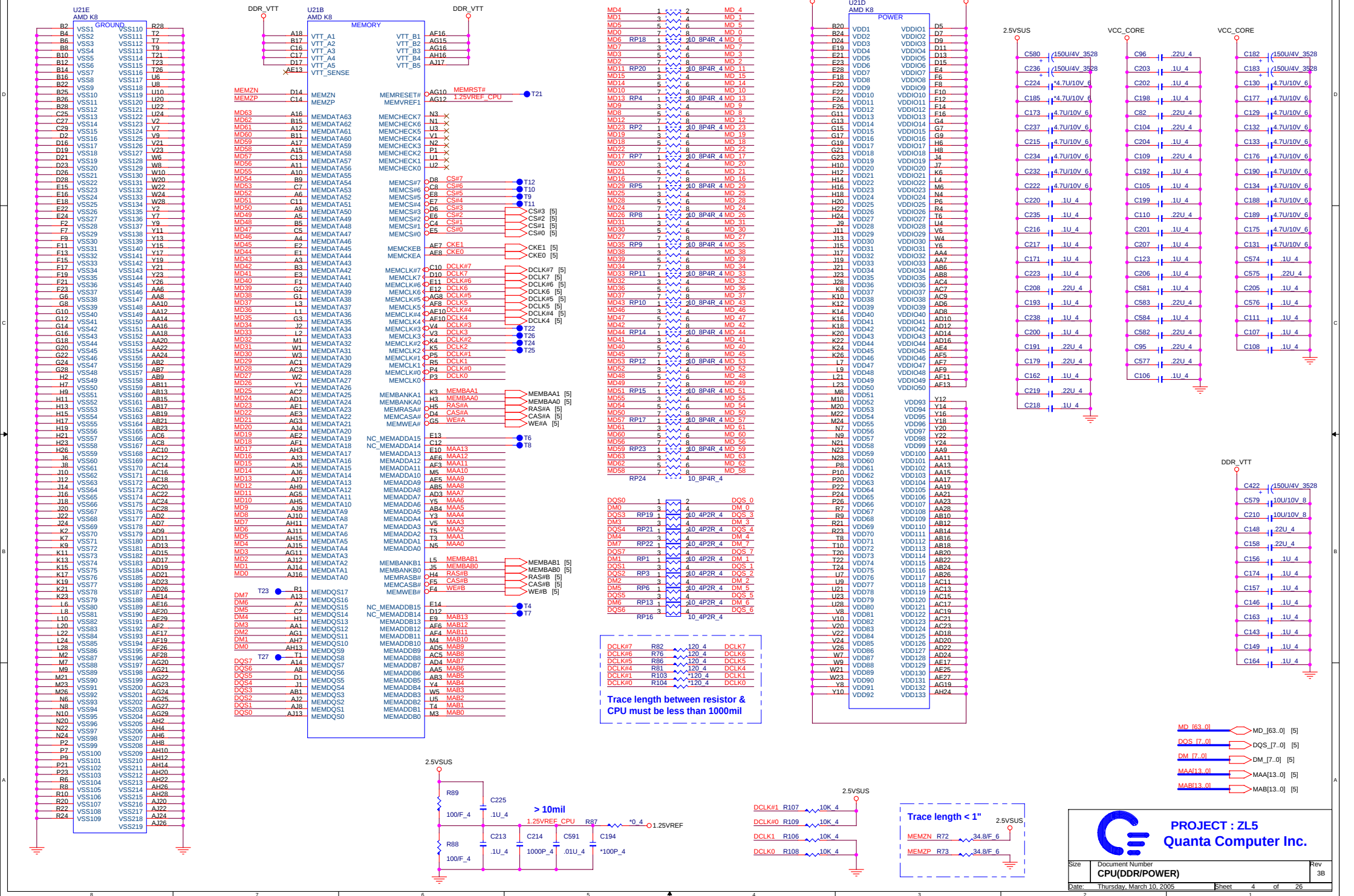
CLK Table for SiS M760 (Not For ICS ICS-952801)

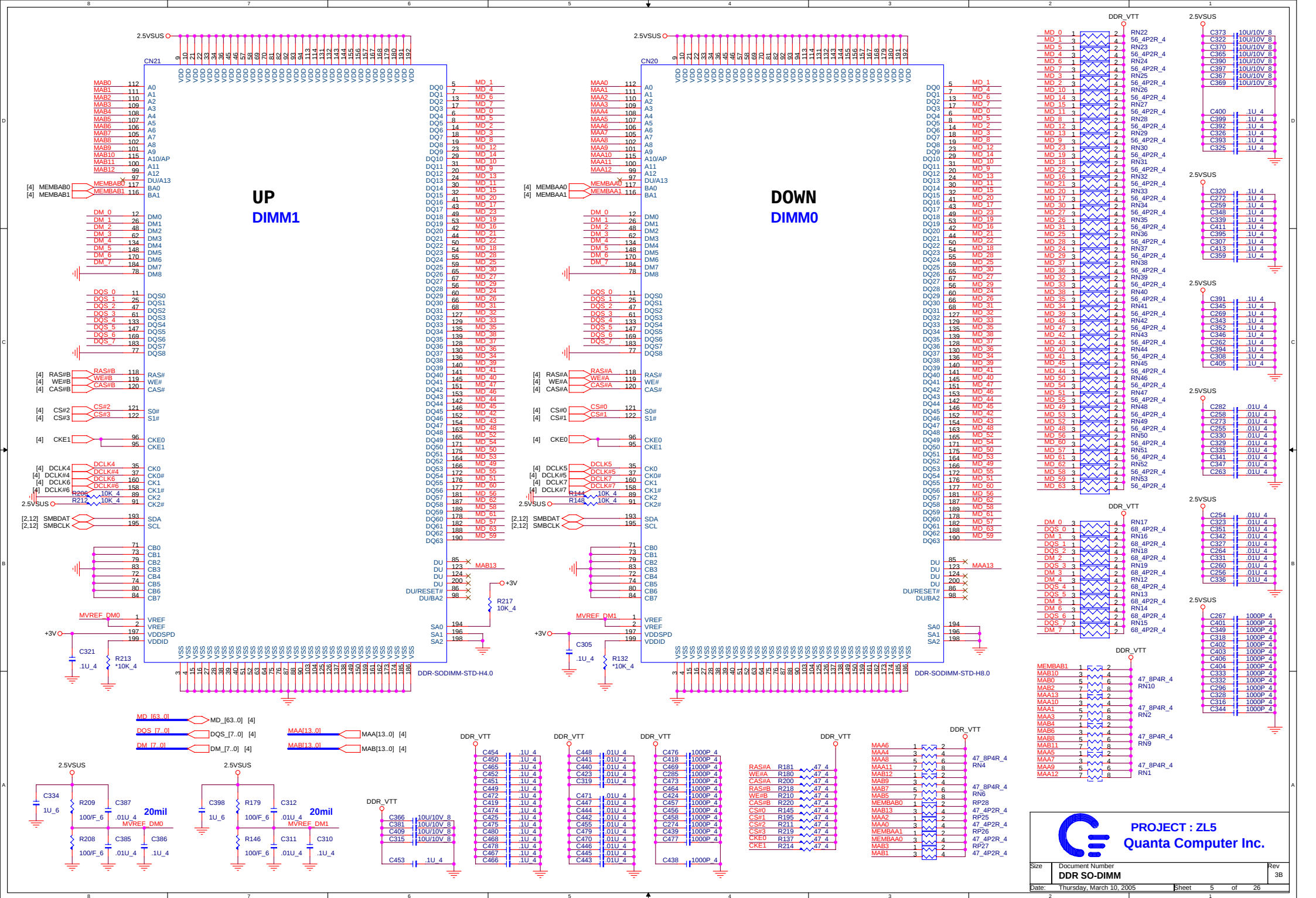
SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

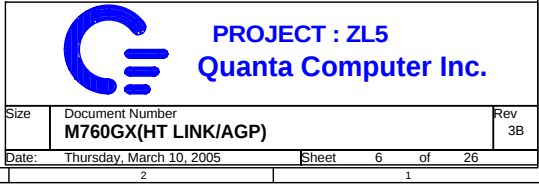
SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
1	0	0	0	0	180	135	67.5	33.75	
1	0	0	0	1	185	132.14	66.07	33.04	
1	0	0	1	0	190	135.71	67.08	33.93	
1	0	0	1	1	195	130	65	32.5	
1	0	1	0	0	205	136.66	68.33	34.17	
1	0	1	0	1	210	140	70	35	
1	0	1	1	0	215	129	64.5	32.25	
1	0	1	1	1	220	132	66	33	
1	1	0	0	0	66.66	66.66	66.66	33.33	
1	1	0	0	1	66.66	100	66.66	33.33	
1	1	0	1	0	100	100	66.66	33.33	
1	1	0	1	1	100	133.33	66.66	33.33	
1	1	1	0	0	133	100	66.66	33.33	
1	1	1	0	1	133	133.33	66.66	33.33	
1	1	1	1	0	166	100	66.66	33.33	
1	1	1	1	1	166	133.33	66.66	33.33	



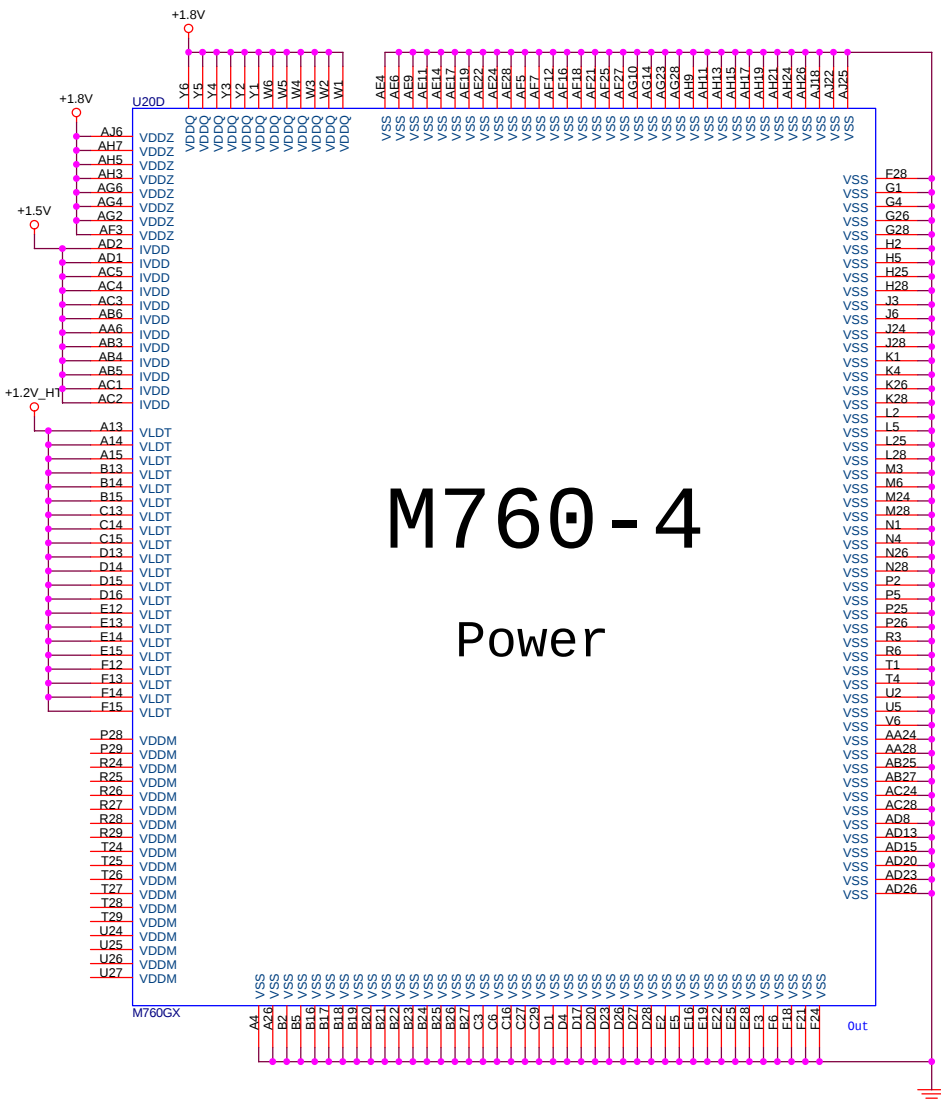
CPU DDR/POWER I/F





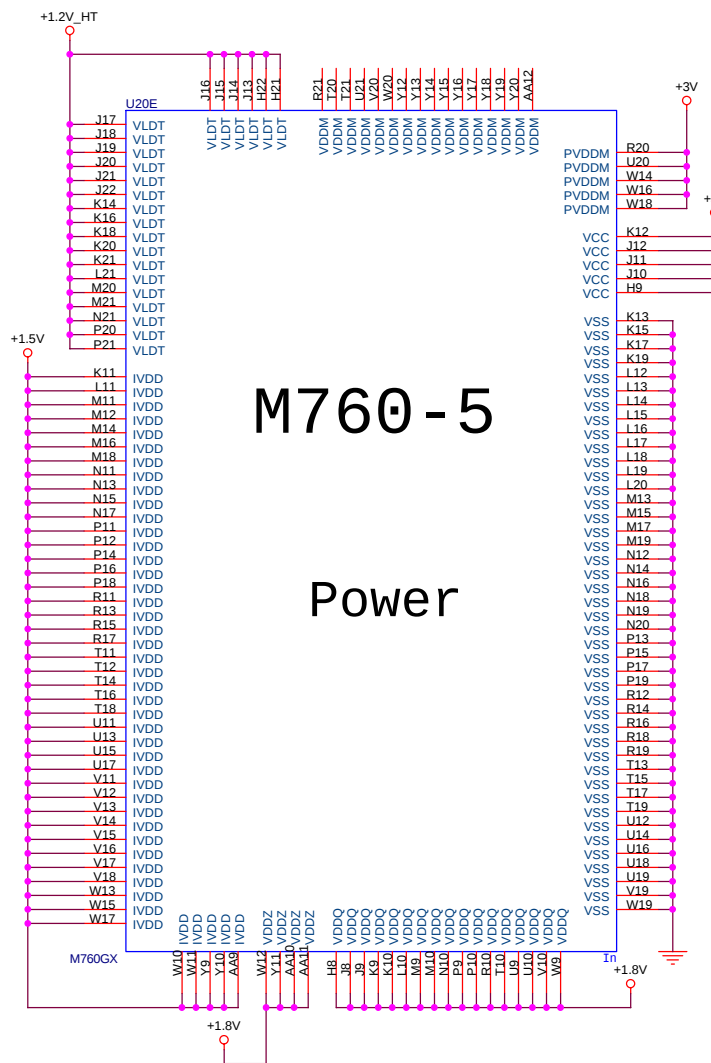


If Support SiS M760LV IVDD=1.5V



M760-4

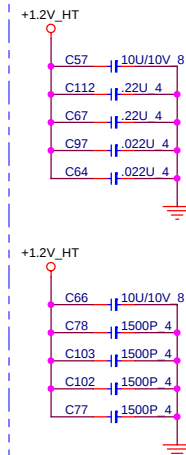
Power



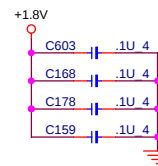
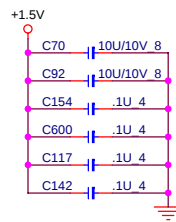
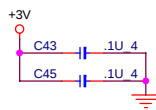
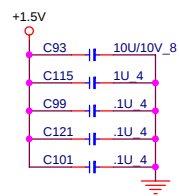
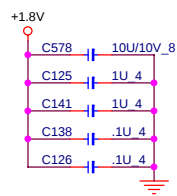
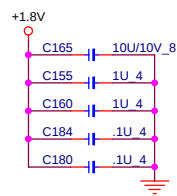
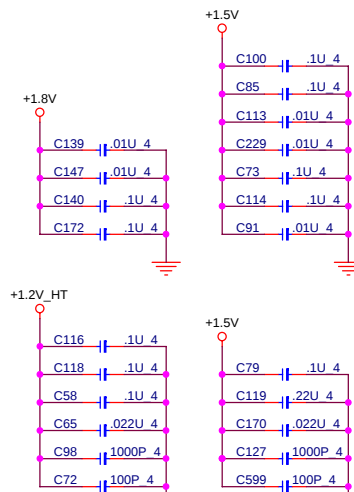
M760-5

Power

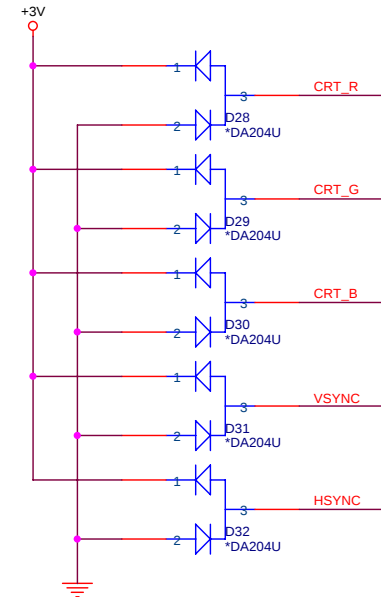
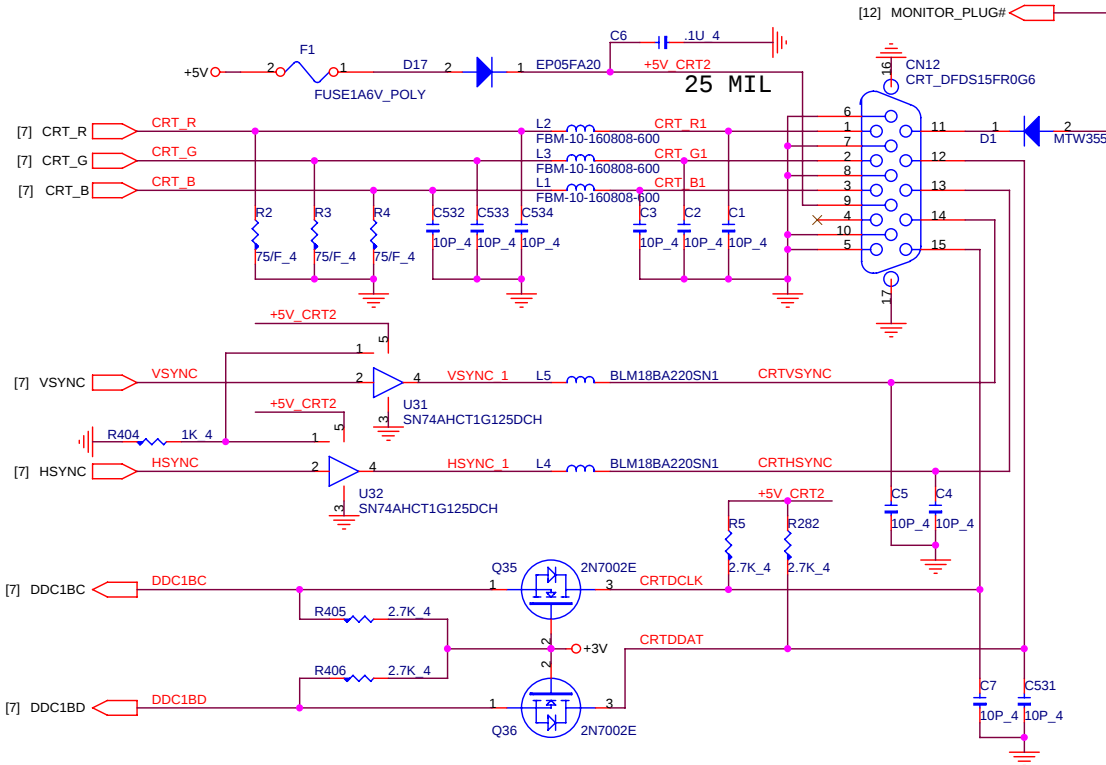
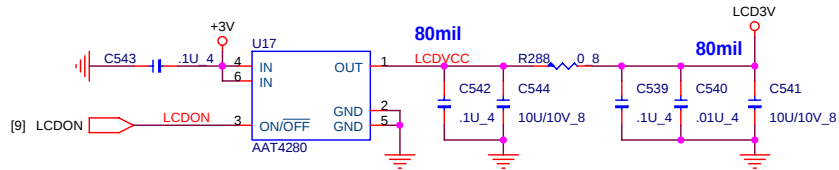
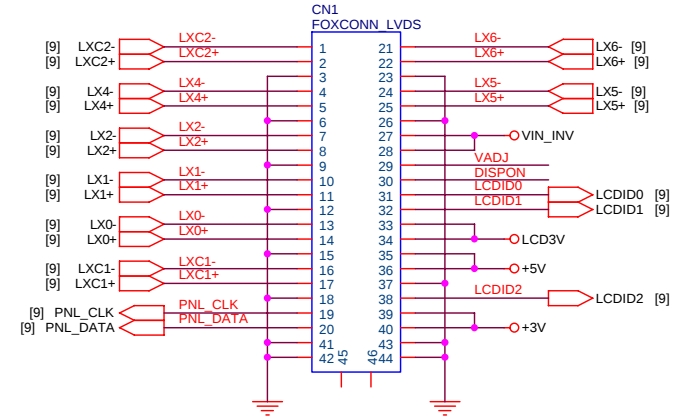
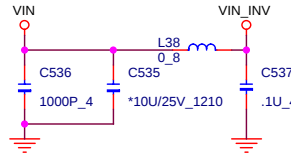
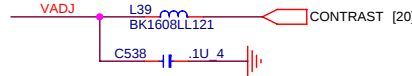
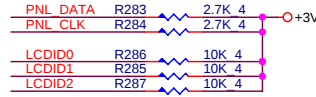
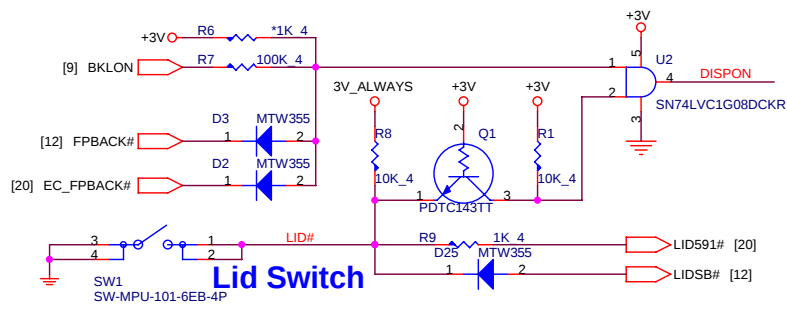
LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.

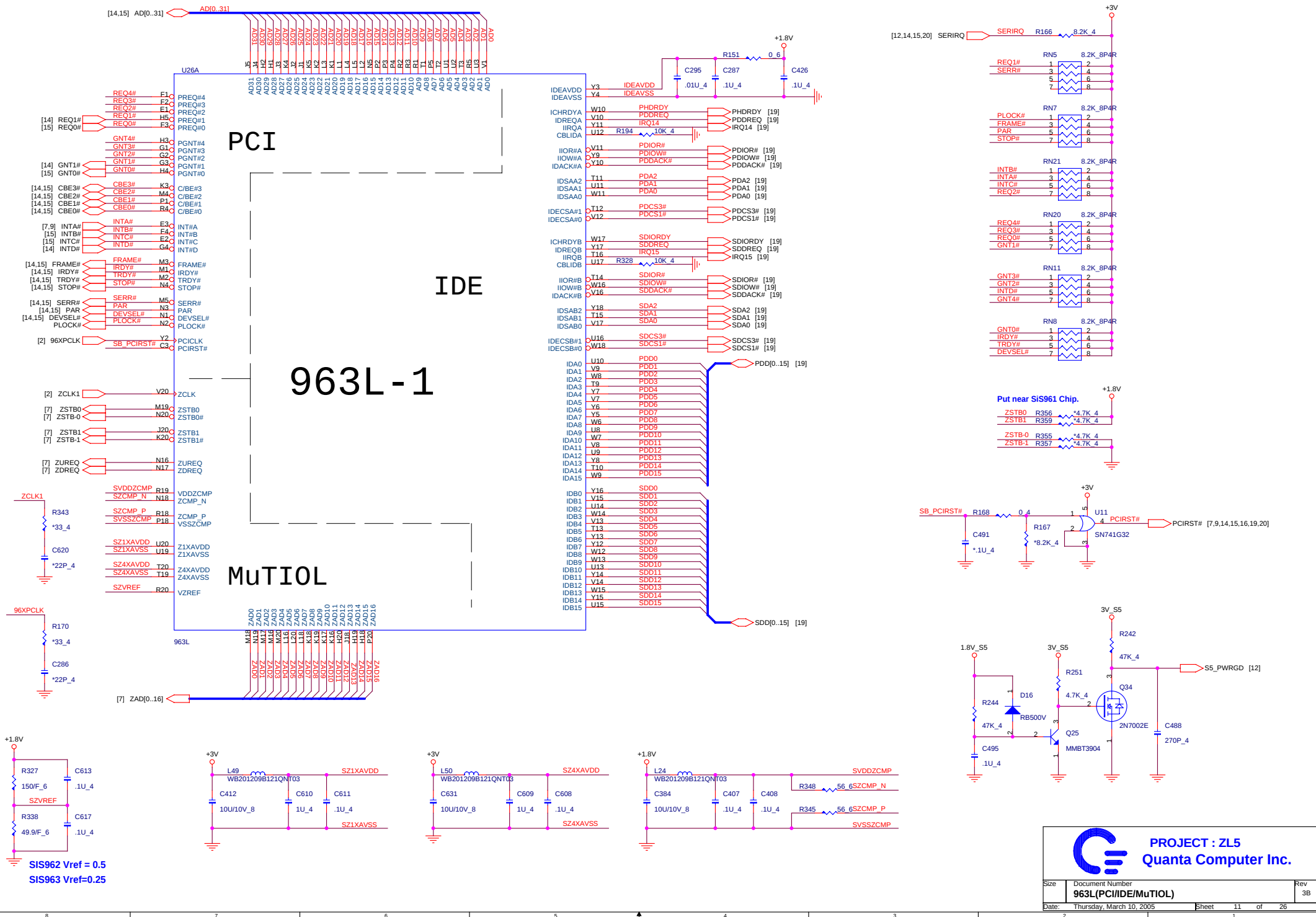


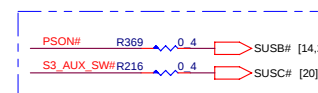
Place these capacitors under 760 solder side.

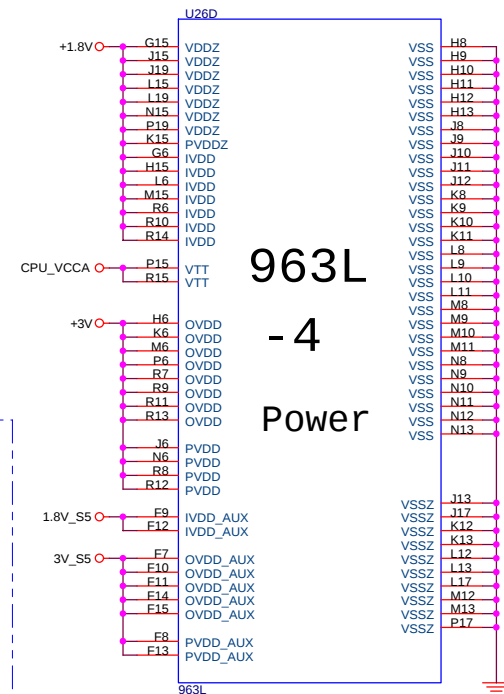
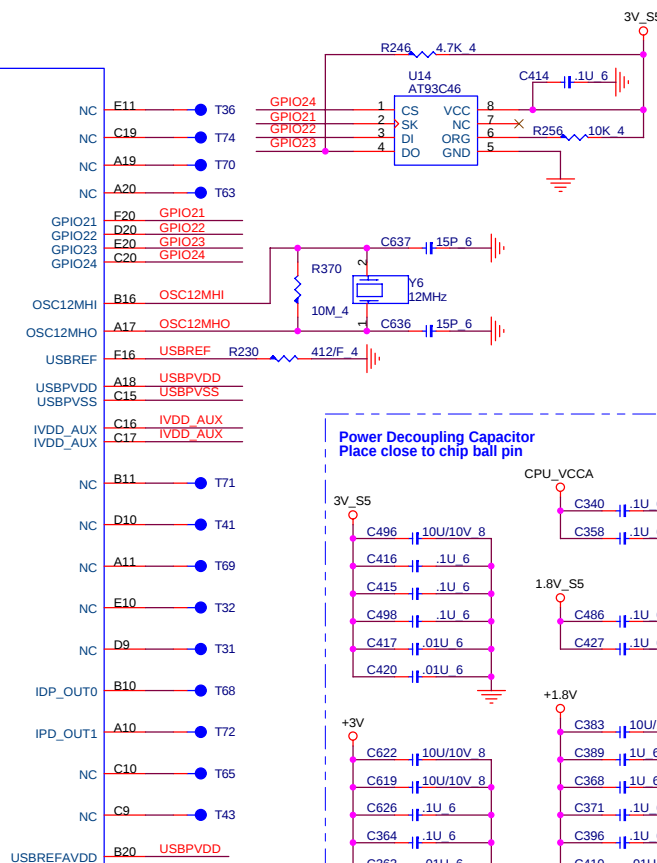
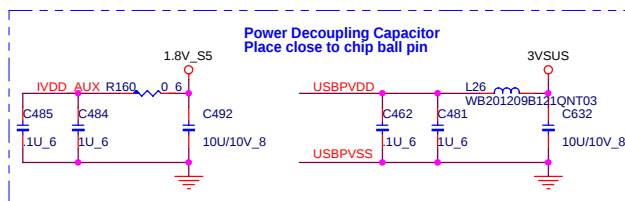
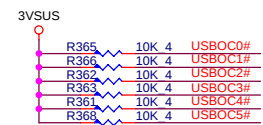
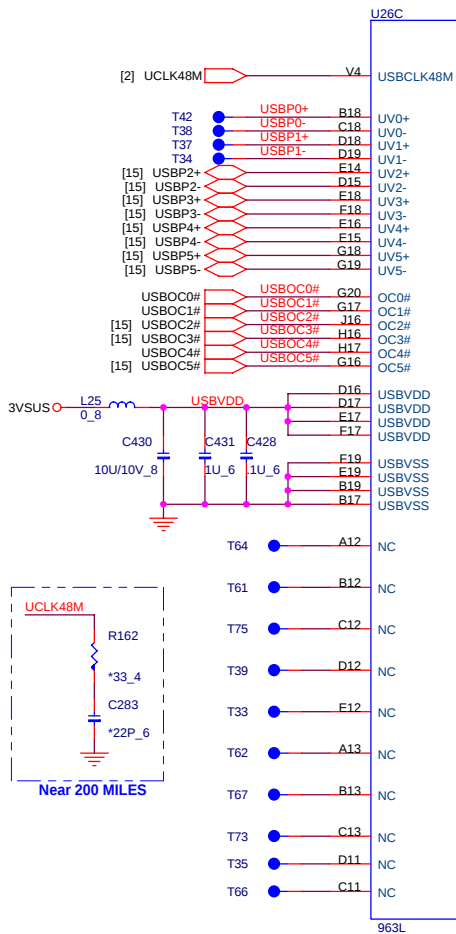


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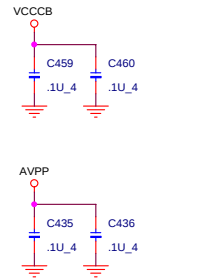
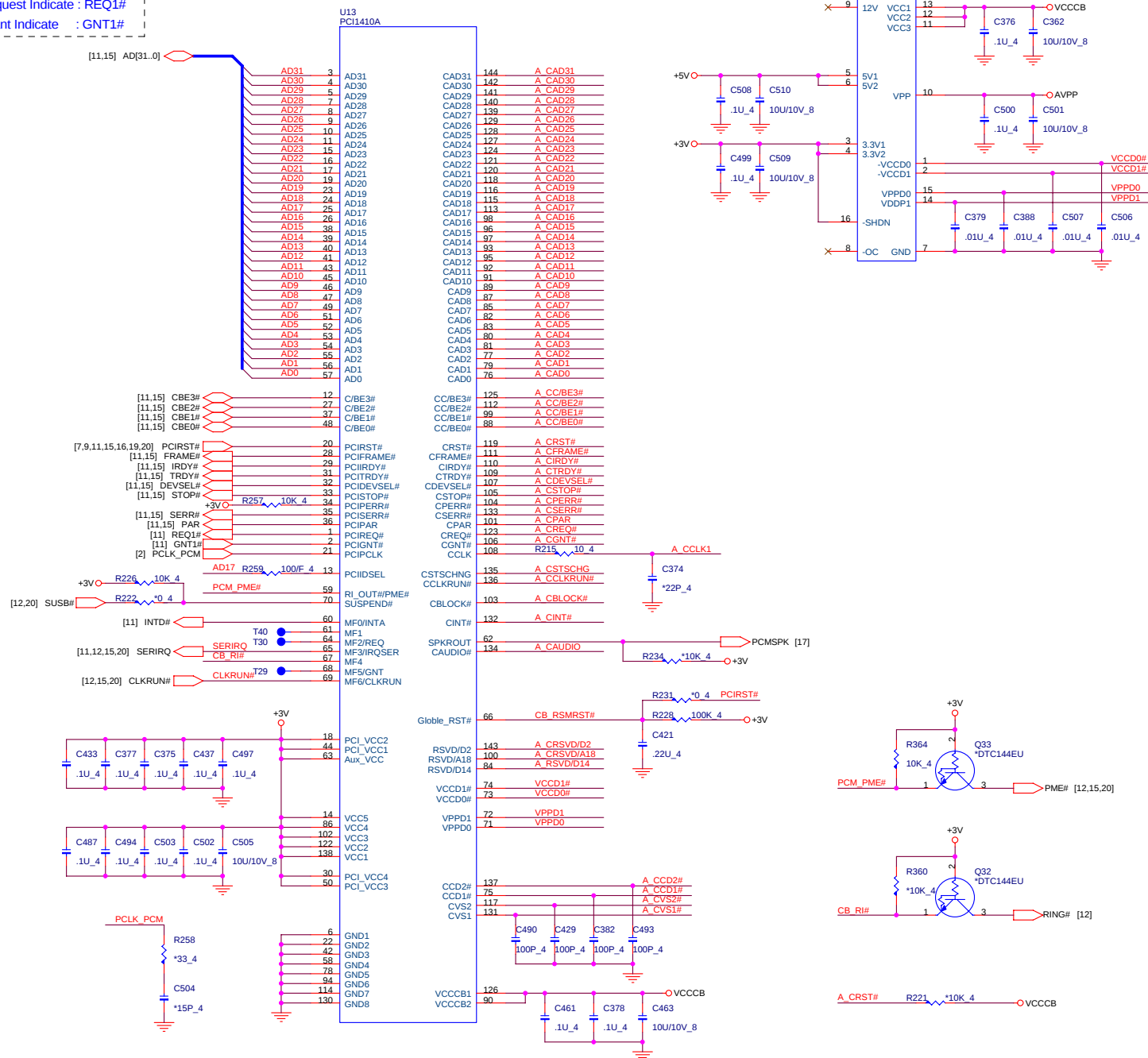




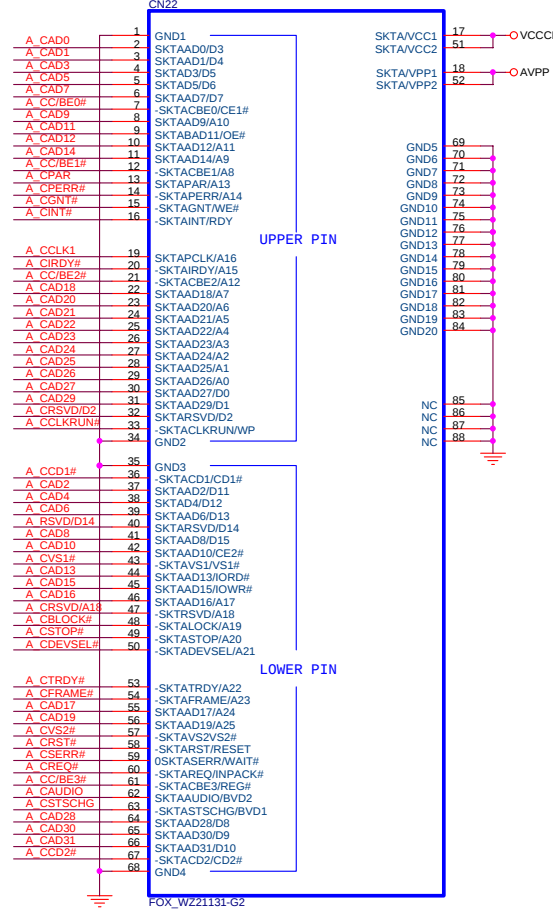




ID Select : AD17
Interrupt Pin : INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#

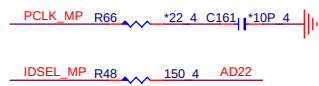


CARDBUS SLOT

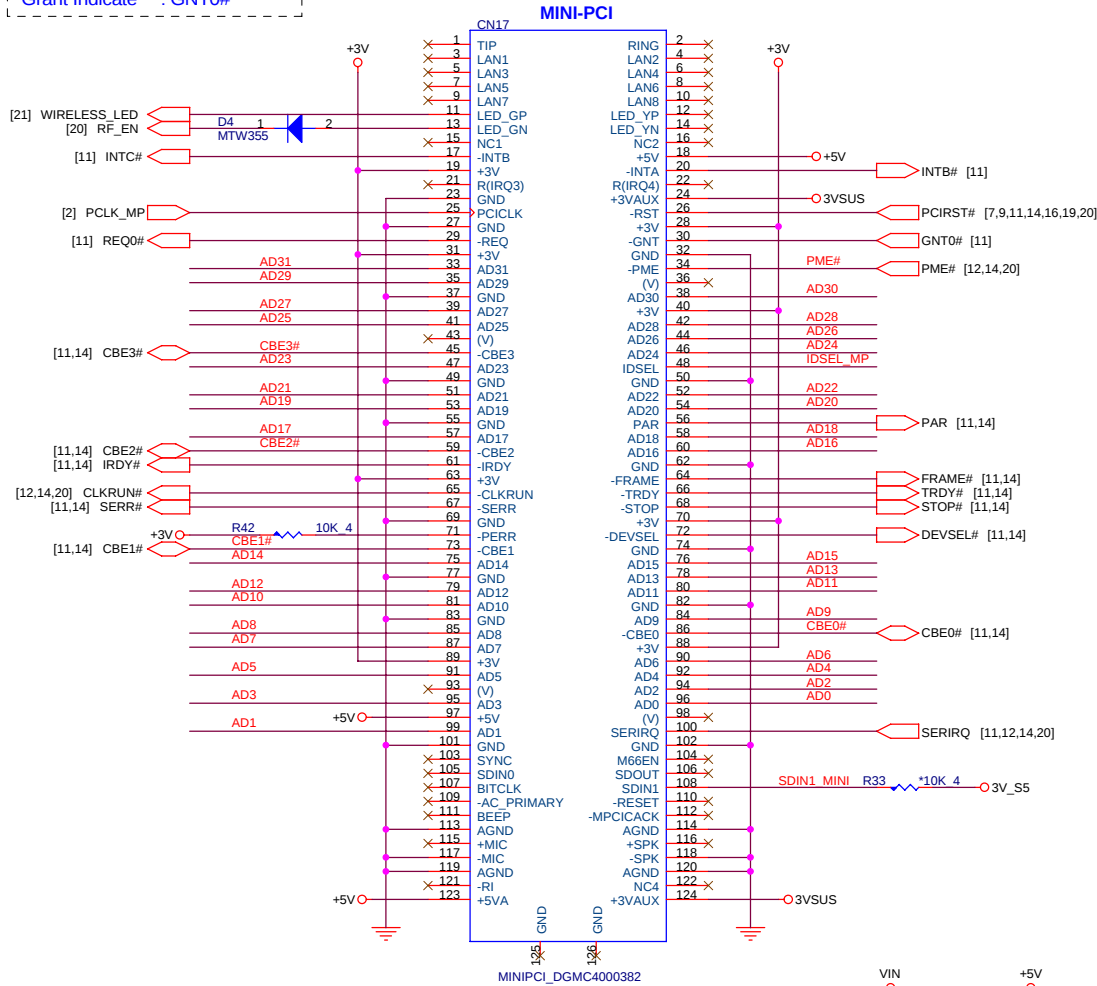


PROJECT : ZL5
Quanta Computer Inc.

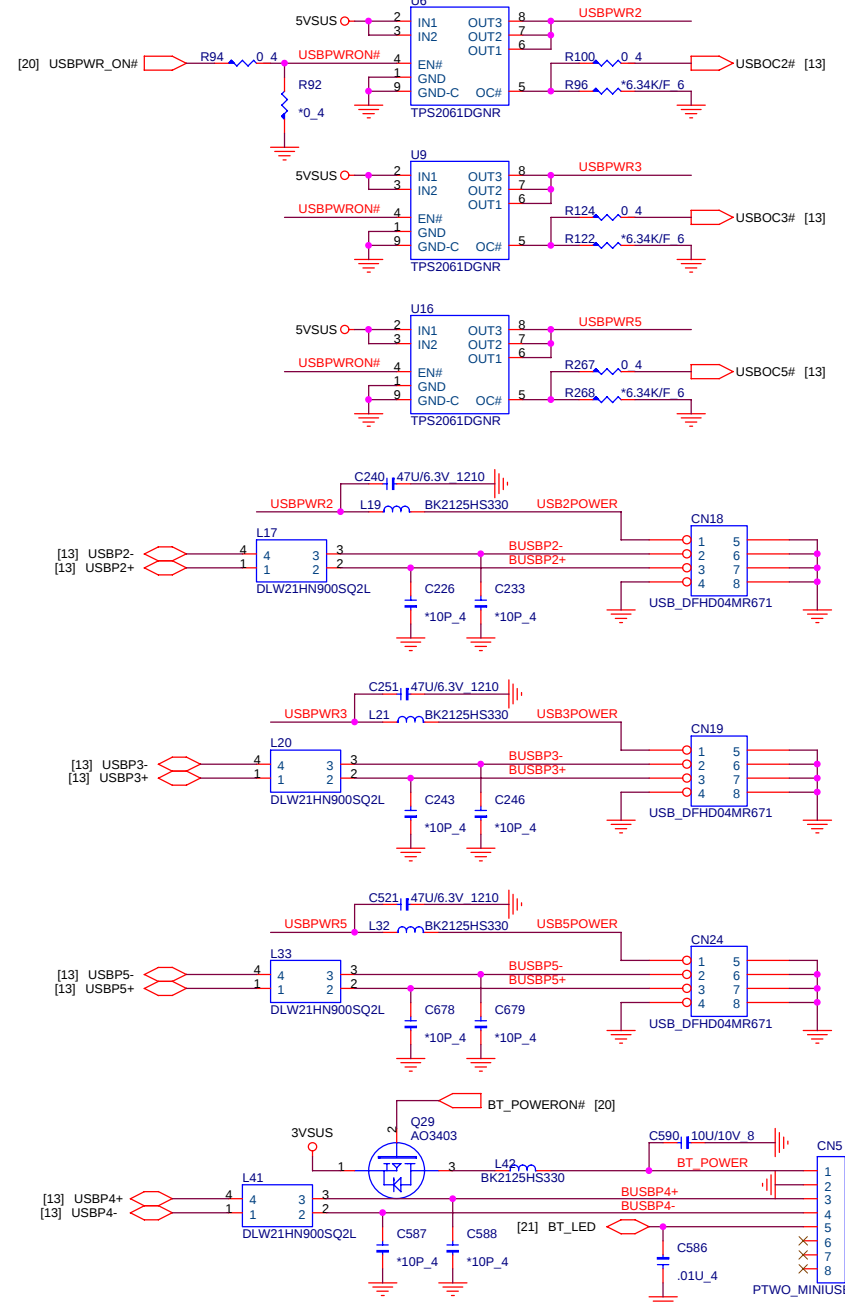
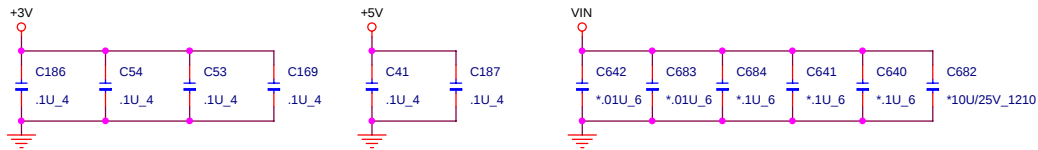
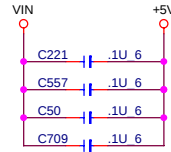
ID Select : AD22
 Interrupt Pin : INTB# , INTC#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#



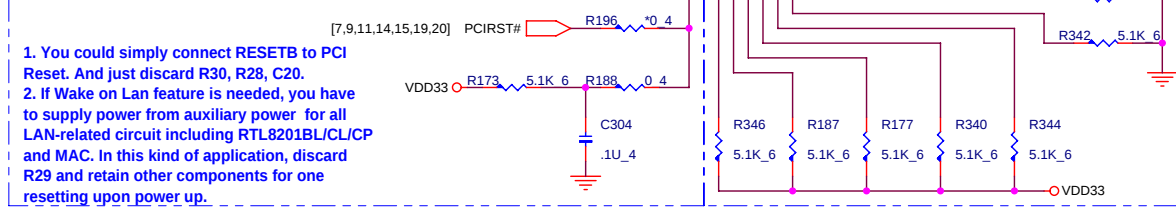
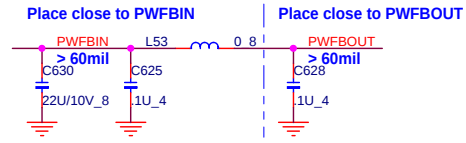
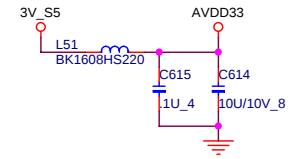
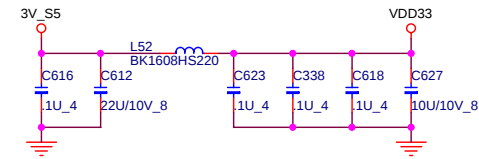
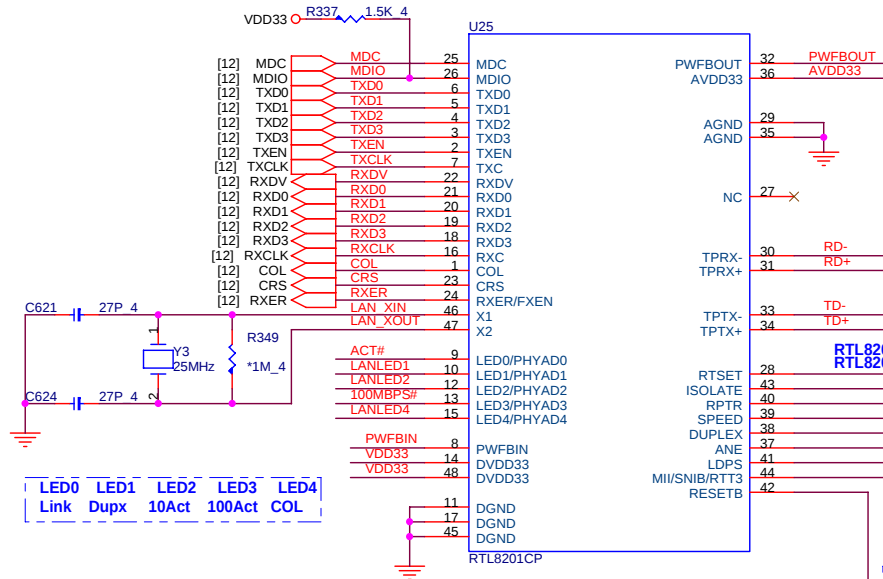
[11,14] AD[0..31] ADIO_311



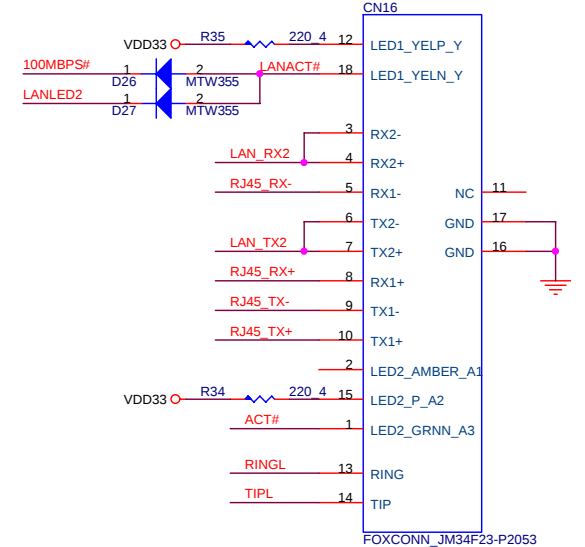
MINIPCI_DGMC4000382



PROJECT : ZL5
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1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.

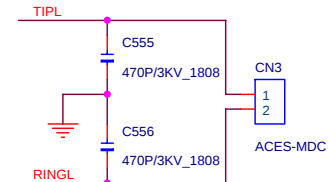
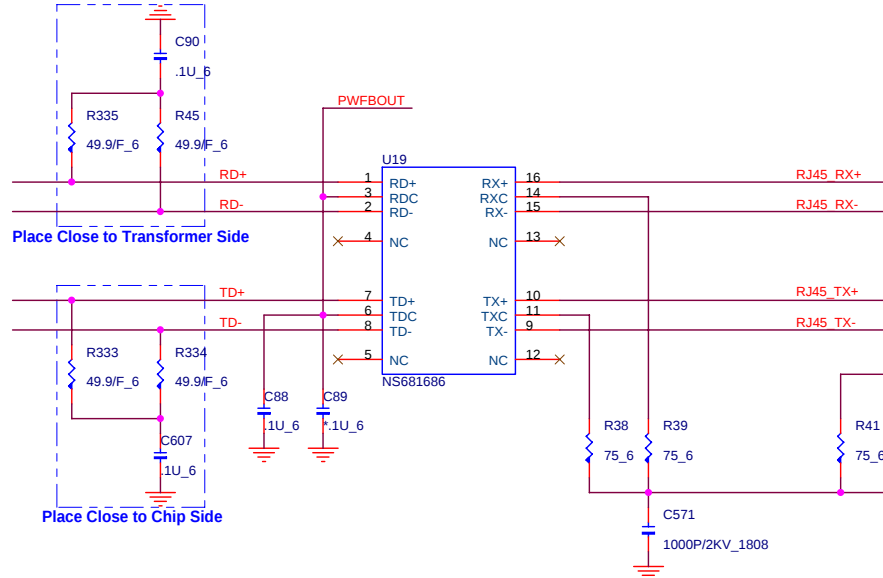


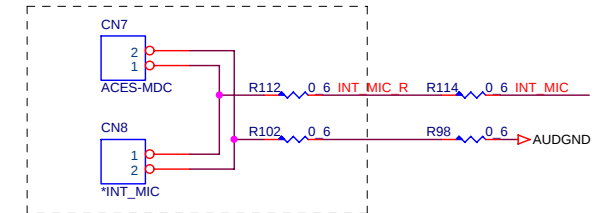
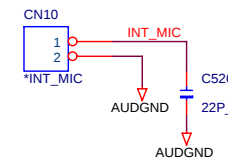
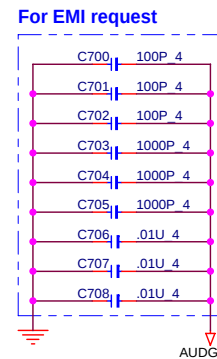
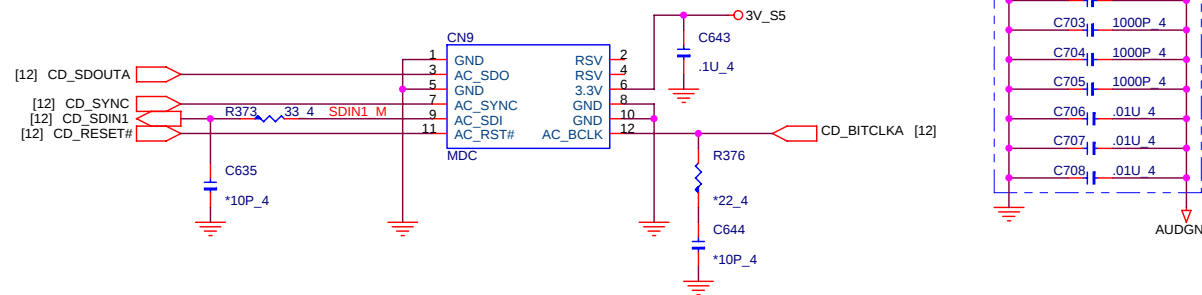
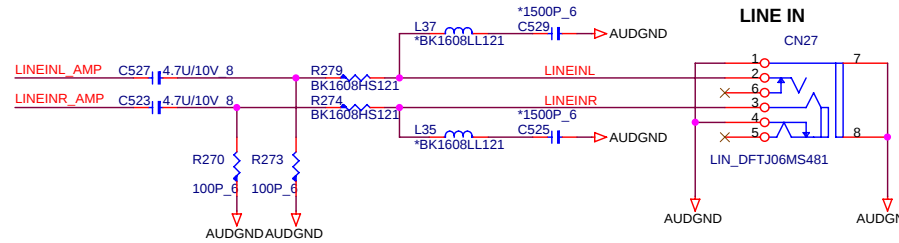
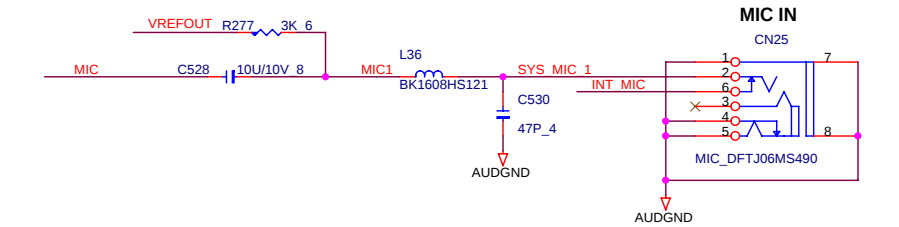
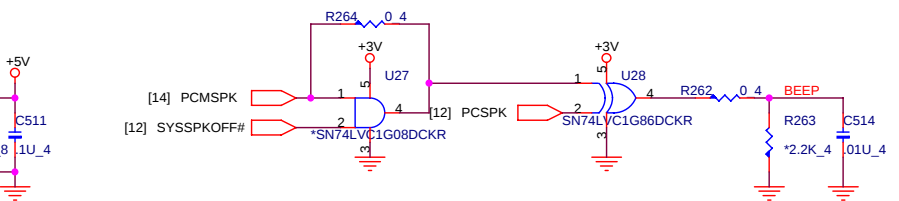
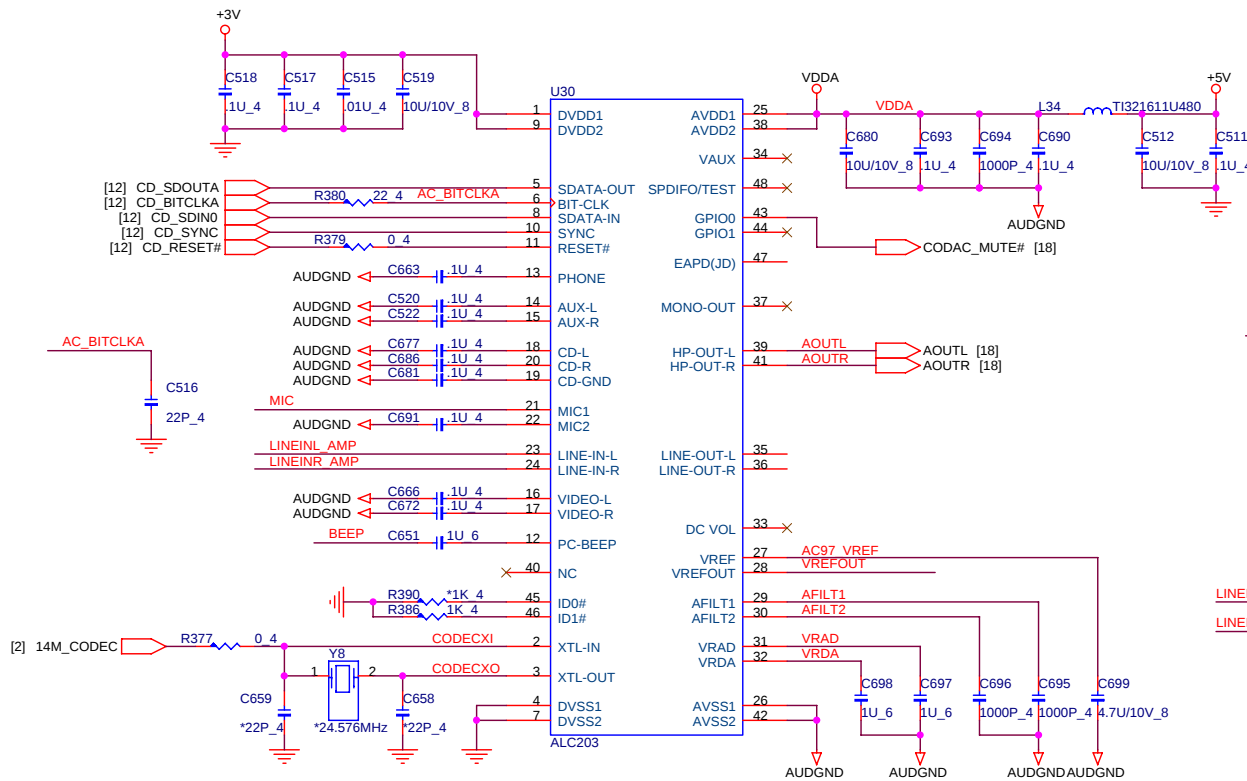
Reserved for 8201CL/CP LED Mode Change to compatible with BL
COL R354 5.1K 4 VDD33

Reserved for ensuring 8201BL/CL/CP latch to UTP Mode.
RXER R339 5.1K 4

Reserved for ensuring 8201CL/CP latch to normal operation mode.
CRS R341 5.1K 4

ACT# R351 5.1K 4 VDD33
100MBPS# R350 5.1K 4
LANLED2 R353 5.1K 4
LANLED1 R352 5.1K 4
LANLED4 R347 5.1K 4



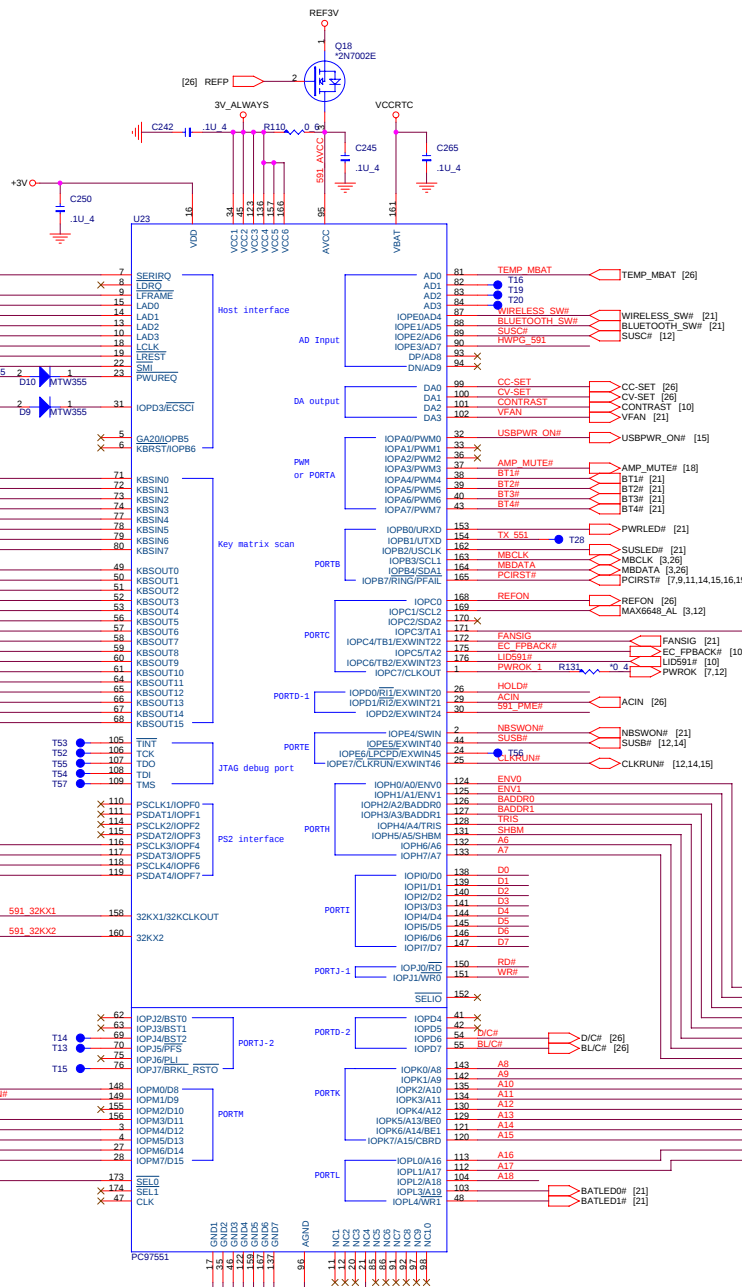
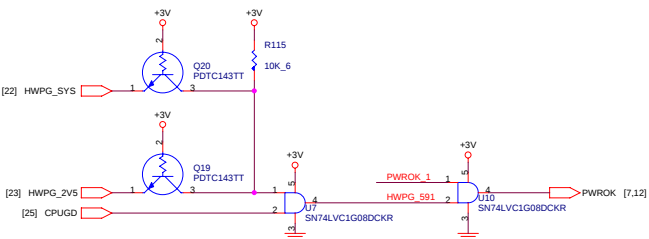
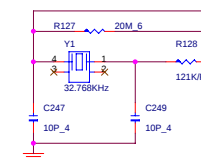
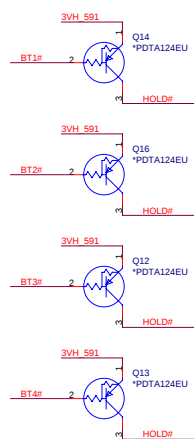
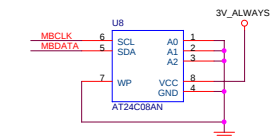




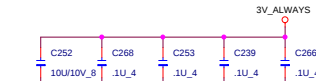
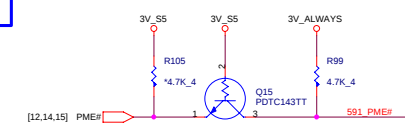
PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	CODEC(ALC203)/MDC1.5	3B
Date:	Thursday, March 10, 2005	Sheet 17 of 26

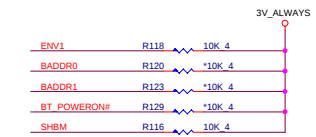
PCLK 591 R117 *22 4 C248 *10P 4



C244 10U_6 FOR 97551 ONLY

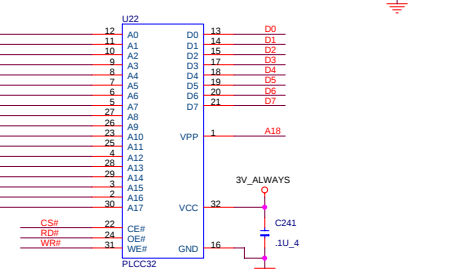
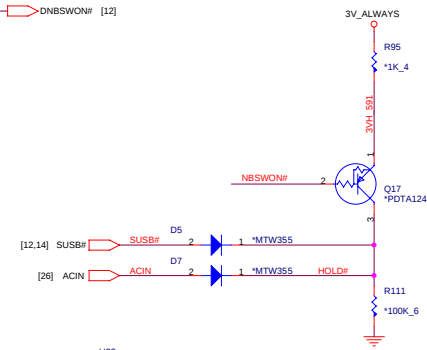
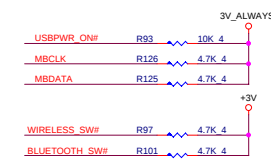


Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

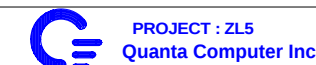


SHBM=1: Enable shared memory with host BIOS

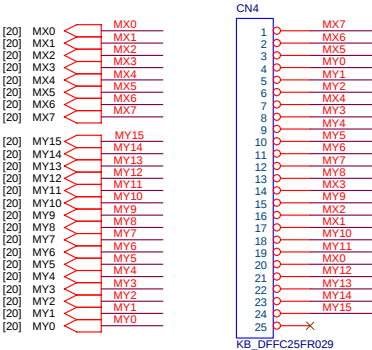
I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+
1 1	Reserved	



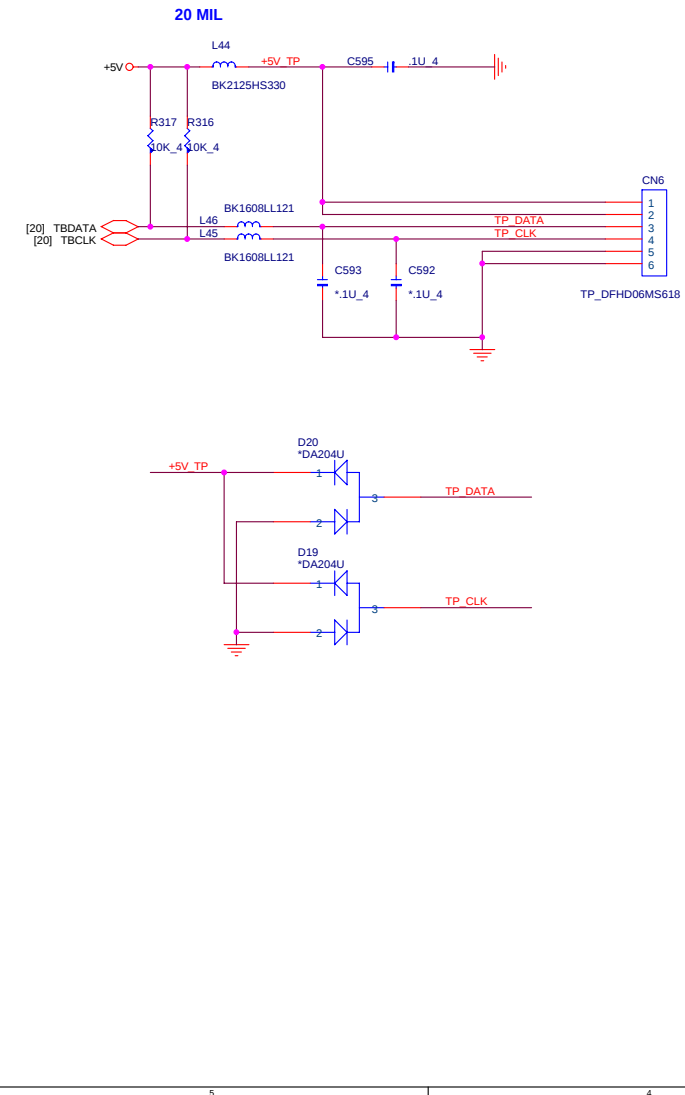
BIU configuration should match flash speed used



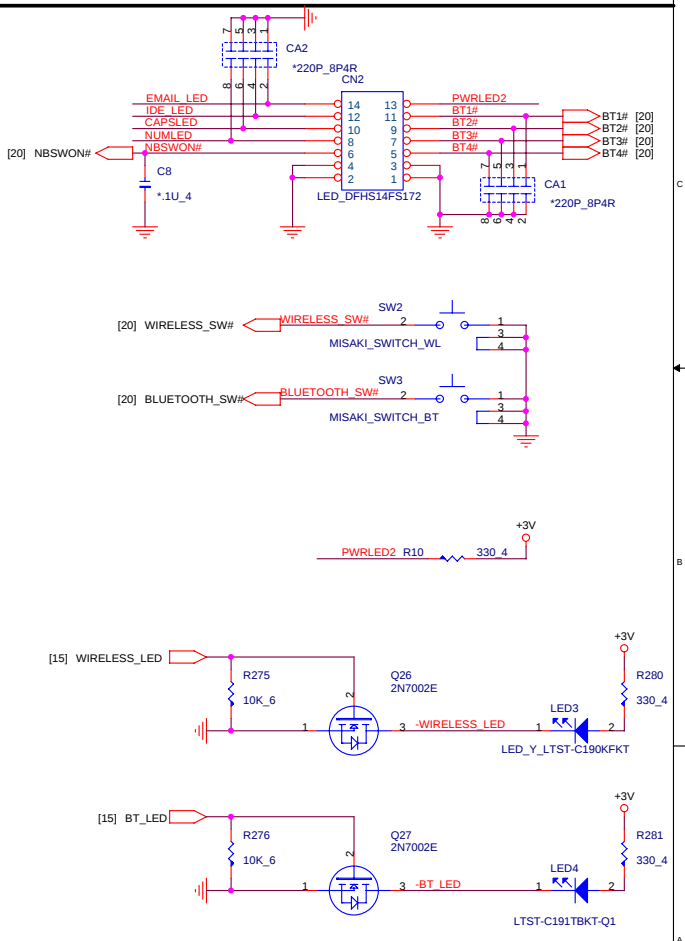
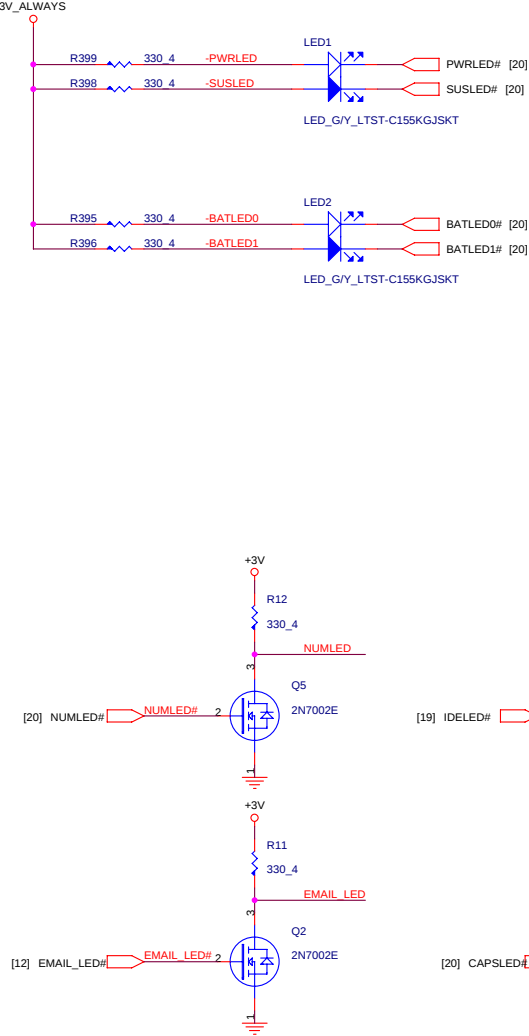
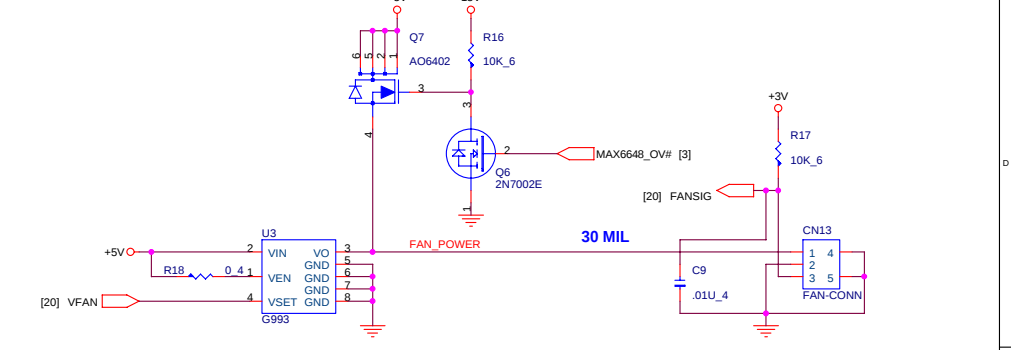
INT K/B

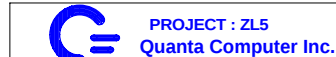


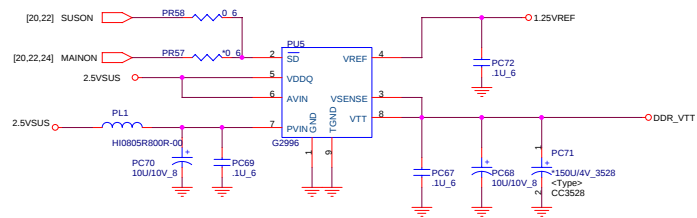
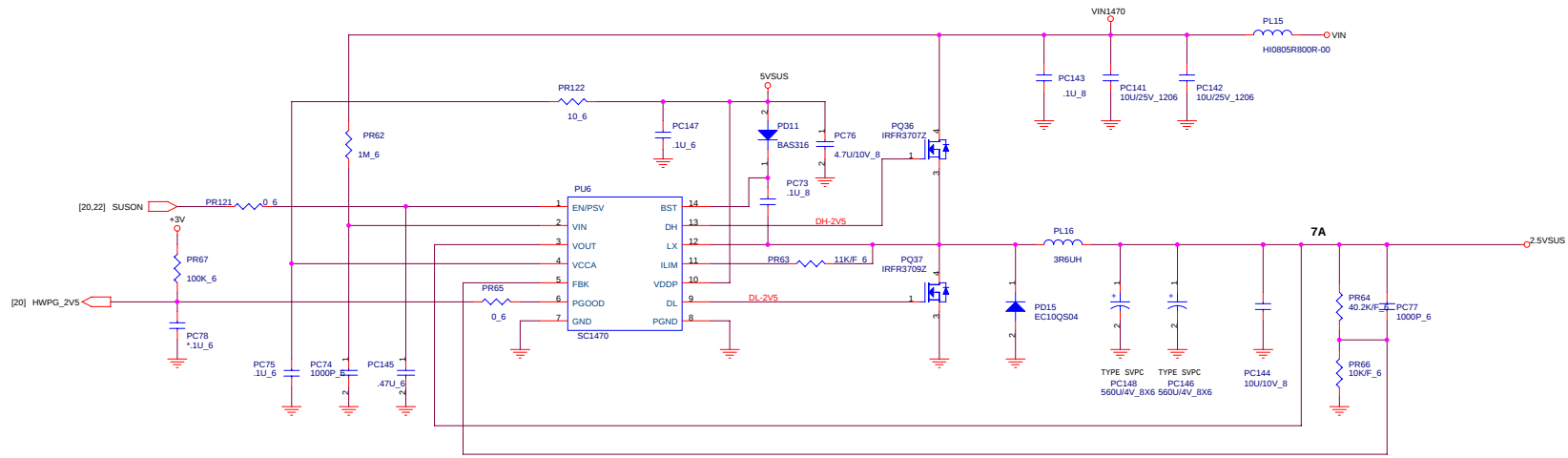
TOUCH PAD



FAN CONTROL

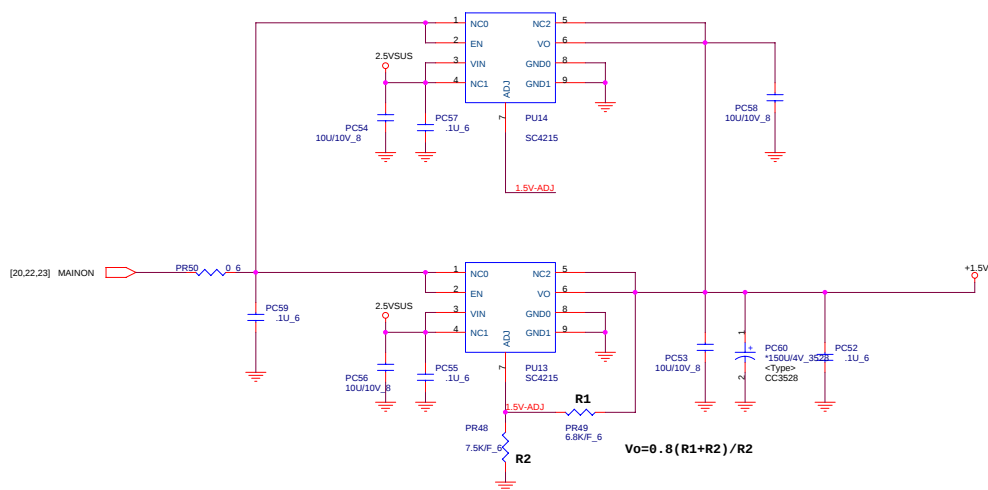
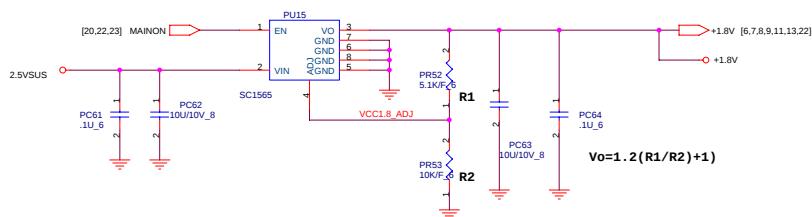
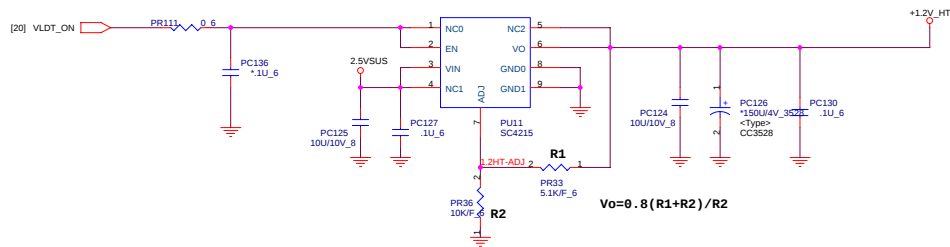






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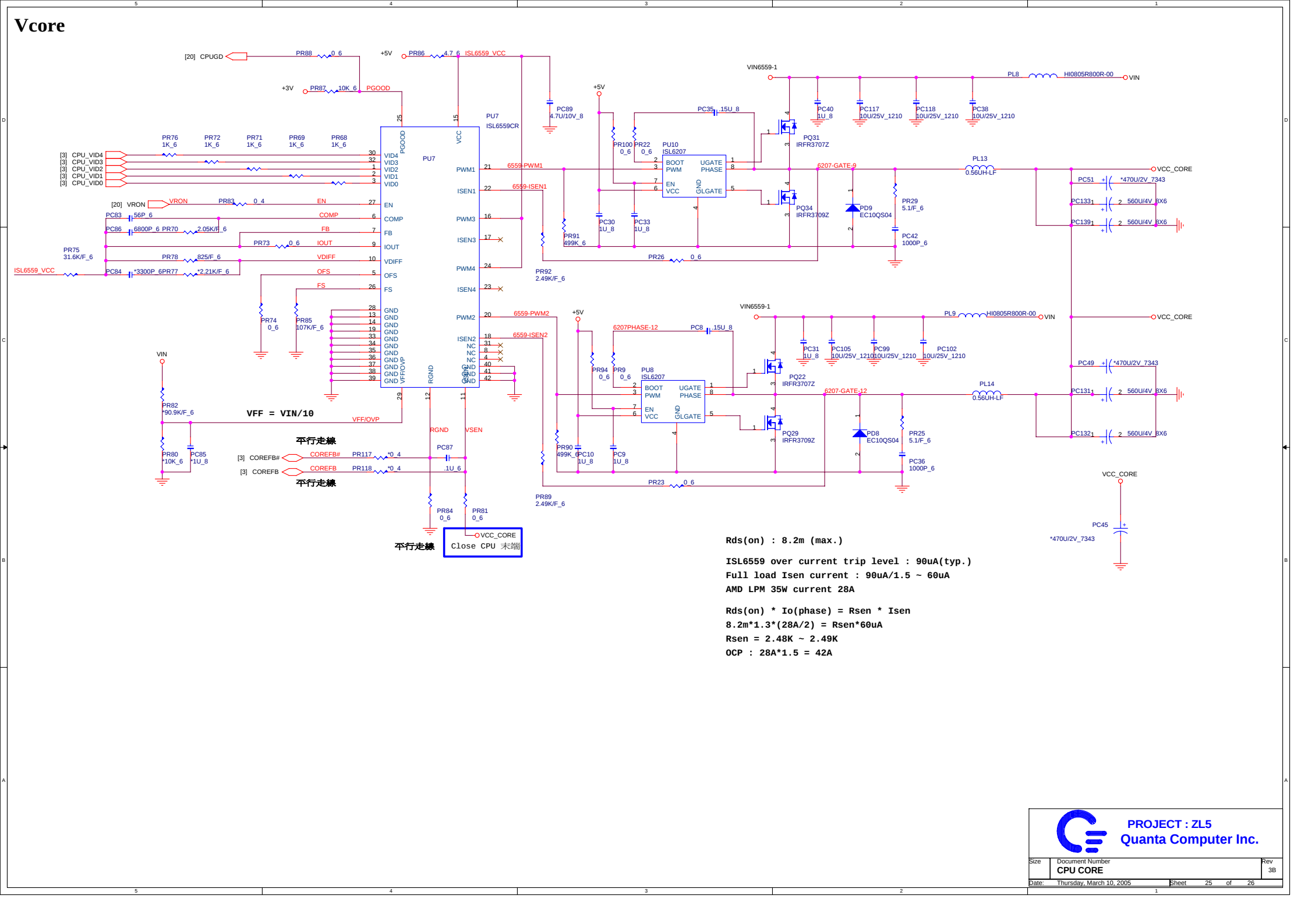
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	2.5VSUS+1.25TERM	3B
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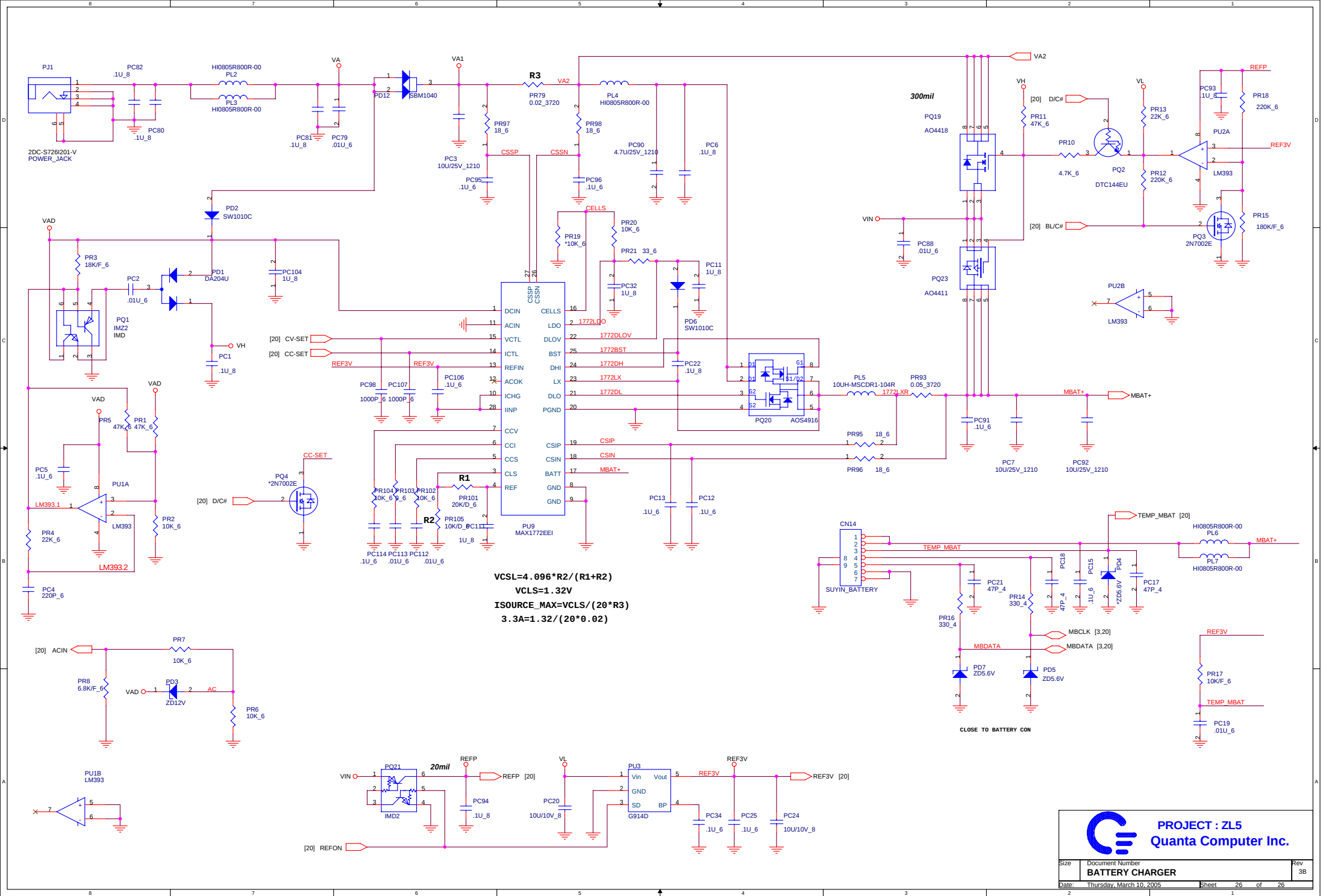
PROJECT : ZL5
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Size	Document Number	Rev
	+1.5V/+1.8V/+1.2V	3B
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